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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,320	11/17/2003	Guillermo J. Rozas	TRAN-P156	5239

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EXAMINER	
ODOM, CURTIS B	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
07/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/25/08 have been fully considered but they are not persuasive. Applicant states (see page 10 of the Remarks) **"In contrast, the Yang (U. S. Patent No. 6, 553, 472) reference requires the initial programming input and based upon that input, calibrates and adjust timing of the device. Applicant reiterates that a process requiring user input, or a process requiring a programmer to set initial parameters of multiple signals for the device is not automatically calibrating as in the claimed invention. Furthermore, independent Claims 1, 7, and 12 specifically recite the automatic adjusting of the claimed invention is free of user input."**

However, it is the understanding of the Examiner that even though the initial parameters are set by a user input, the timing (delay) parameters "automatically" adjust based on the initial parameters using the functions/equations as described in Yang, column 5, line 32-column 6, line 19.

The Applicant further states (see page 11 of Remarks) **"Accordingly, Applicant asserts that Yang (or Johnson, US 20030122696) does not show the calibration for both data write transactions and data read transactions as in the claimed invention. Similar limitations are included in each of the independent Claims 7, 12, 18, and 22. Additionally, automatic calibrating and automatic adjusting limitations are included in each of the independent Claims 1, 7, 12, 18, and 22."**

However, Yang et al. discloses calibration (adjustment) of timing relationships (using delays) between signals from the MC to the SDRAM for both read and write operations (see column 5, line 32-column 6, line 19).

The Applicant also states (see page 12 of the Remarks) "**Furthermore, applicant points out that Claims 12 and 18 explicitly recites the calibration as taking place without requiring a valid initial operating point within the specified operating parameters for the DRAM component. Applicant points out that the cited section of Yang (e.g., Yang column 2 lines 30-39) does not say anything about inoperative DRAM components. Applicant further point out that the DRAM component as envisioned by Yang must at least be operative to some extent in order to accept and receive the "initialization parameters". There is no disclosure or teaching within Yang of the finding of some parameters within an envelope that can support some functional capability of an otherwise nominally inoperative DRAM component. In contrast, such conditions are explicitly recited as within the capabilities of the present invention.**"

It is the understanding of the Examiner that claims 12 and 18 recite adjustment (calibration) taking place without requiring a valid initial operating point within a the specified operating parameters. Thus, to the understanding of the Examiner, claims 12 and 18 recite the calibration does not need a specific operating point to begin calibration; the calibration can begin at any operating point within specified parameters. The Examiner would like to point out that these claims do not recite anything about inoperative DRAM components (wherein inoperative DRAM components are recited in claim 22 and properly rejected), rather the claims simply describes an initial operating point for the DRAM is not required. Furthermore, Yang discloses a

valid initial operation point is not required since the controller has the ability to calculate delays and set its own variable initialization point that offers the optimum system performance (see column 2, lines 30-39).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 7, 8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008).

Regarding claim 1, Yang et al. discloses a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit component;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

for both read and write transactions, automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the integrated circuit device.

Yang et al. does not disclose the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Regarding claim 2, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 3, Yang et al. further discloses adjusting a timing (phase) relationship is performed by a memory controller (Fig. 2, block 31, see column 6, lines 20-25) coupled to the SDRAM.

Regarding claim 7, Yang et al. discloses a system (see Fig. 2) for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals by implementing programmable time delays (see column 3, lines 10-23) for an integrated circuit device SDRAM), comprising:

a controller (Fig. 2, block 31) for generating command signals (see column 3, lines 36-43) for accessing an integrated circuit component;

a delay calibrator of programmable delays (see column 5, line 31-column 6, line 25 and column 8, lines 41-67) integrated within the controller (see column 6, lines 20-25) for accessing data signals (see column 3, lines 36-43) for conveying data for the integrated circuit device and for accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67), for both read and write transactions, the delay calibrator configured to automatically adjust a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19 and column 8, lines 41-67) to calibrate (optimize) operation of the integrated circuit device, wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not disclose a valid initial operation point that exists within specified operating parameters is not required and wherein the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships

between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a valid initial operation point that exists within specified operating parameters or a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Regarding claim 8, Yang et al. further discloses the circuit device is an SDRAM (see column 3, lines 10-23).

Regarding claim 12, Yang et al. discloses a method for finding an initialization point in a SDRAM (see column 2, lines 30-39) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

for both read and write transactions, automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM

and find an optimal initialization point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not disclose a valid initial operation point that exists within specified operating parameters is not required and wherein the automatic adjusting is free of user input. However, Johnson et al. discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a valid initial operation point that exists within specified operating parameters or a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

4. Claims 4-6, 9-11, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in Office Action 1/25/2008) as applied to claims 2, 8, and 12, and in further view of Suzuki (previously cited in Office Action 1/8/2007).

Regarding claims 4-6, 9-11, and 15-17, Yang et al. and Johnson et al. do not specifically disclose the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to enable both reading and writing for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. and Johnson et al. with the DDR SDRAM of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

Regarding claim 18, Yang et al. and Johnson et al. disclose all the limitations of claim 18 (see rejection of claim 12), including the operations of the SDRAM written as software (see Yang et al., column 2, lines 11-16). Yang et al. and Johnson et al. do not specifically disclose the calibrated SDRAM is a DDR SDRAM, the data signals comprise a plurality of DQ signals, or the sampling (clock) signals comprise a plurality of DQS signals.

However, Suzuki et al. also discloses a memory controller (see Fig. 1, block 1100) which controls a DDR SDRAM (see Fig. 1, block 1000), and provides both continuous data (DQ) signals and data strobe (DQS) signals to the DDR-SDRAM to determine both reading and writing operations for the DDR-SDRAM (see sections 0029-0030). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the SDRAM of Yang et al. and Johnson et al. with the DDR SDRAM (and DQ and DQS signals for control of the DDR SDRAM) of Suzuki since Suzuki states the DDR (double data rate) SDRAM provides higher frequency operation (than that of the SDRAM), see section 0004.

5. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in

Office Action 1/25/2008) as applied to claim 12, and in further in view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 13 and 14, Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al and Johnson et al. do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al. and Johnson et al. with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

6. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Johnson et al. (previously cited in

Office Action 1/25/2008) in view of Suzuki (previously cited in Office Action 1/8/2007) as applied to claim 18, and in further view of Keeth (previously cited in Office Action 1/8/2007).

Regarding claims 19 and 20 (see above rejection of claim 18), Yang et al. discloses configuring the memory controller to operate with the DRAM in accordance with an optimal operating mode (see column 6, lines 20-25). Yang et al., Johnson et al., and Suzuki do not disclose the time delay operation involves performing a coarse time delay calibration by altering the timing relationship in accordance with a large step interval to find the operating mode of the DRAM component; and performing a fine time delay calibration by altering the phase relationship in accordance with a small step interval to optimize the operating mode of the DRAM component, wherein the optimal operating mode is determined by the fine calibration.

However, Keeth discloses a memory device (see Fig. 1) including a memory controller (see Fig. 1, block 22) coupled to a DRAM (Fig. 1, block 26), wherein minimum and maximum delays from command at the memory controller to read data an the memory controller are accommodated by performing vernier clock adjustments, wherein there is a coarse delay adjustment with a large bit interval and a fine delay adjustment with a smaller interval (within a bit period (see column 4, lines 11-18 and column 7, lines 44-51). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the timing delays of Yang et al., Johnson et al., and Suzuki with the coarse and fine delay as disclosed by Keeth since Keeth states this coarse and fine (vernier) delay adjustment allows data to be accurately clocked in memory devices even at higher data transmission rates (see column 2, liens 46-55).

7. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (previously cited in Office Action 1/8/2007) in view of Davis (previously cited in Office Action 1/8/2007), and in further view of Johnson et al. (previously cited in Office Action 1/25/2008).

Regarding claim 12, Yang et al. discloses in a memory controller, a method for finding an initialization (operating) point in a SDRAM (see column 2, lines 30-39) coupled to a memory controller of a microprocessor chip which represents a printed circuit board (see column 1, lines 19-25) by altering intra-cycle timing relationships between command signals, data signals, and sampling (clock) signals by implementing programmable time delays (see column 3, lines 10-23) for the SDRAM, comprising:

generating command signals (see column 3, lines 36-43) for accessing the SDRAM;

accessing data signals (see column 3, lines 36-43) for conveying data for the SDRAM;

accessing sampling (clock) signals (see column 3, lines 36-43) for controlling the sampling of the data signals based on the rising edge of the clock signal (see column 3, lines 48-67); and

for both read and write transactions, automatically adjusting a phase (timing) relationship in a memory controller by adjusting programmable delays (see column 6, lines 20-25 and column 8, lines 41-67) between the command signals, the data signals, and the clock signals (as described in column 5, line 32-column 6, line 19) to calibrate (optimize) operation of the DRAM and find an optimal initialization point (see column 2, lines 30-39), wherein a valid initial operation point is not required since the controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39).

Yang et al. does not specifically disclose the DRAM component is inoperable at specified initial operating parameters, wherein the automatic altering is performed free of user input.

However, as described above, Yang et al. discloses the memory controller has the ability to calculate delays and set its own initialization point that offers the optimum system performance (see column 2, lines 30-39). Davis further discloses operating points for the DRAM control and data signals wherein the DRAM produces invalid data (or is inoperable), see column 2, lines 30-49). Therefore, it would have been obvious to set an initialization point in Yang et al. when the DRAM produces invalid data as described by Davis since Yang et al. states calculating delays and setting an initialization point offers the optimum system performance (see column 2, lines 30-39).

Johnson et al. further discloses calibrating timing (phase) relationships between control (command) and data signals (see section 0001), wherein calibrating the timing relationships between the data and command clocks also correctly calibrates the sampling (signals) of the data (see section 0006). The calibration takes place at initialization and does not require a user input as described in section 0006. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the calibration of Yang et al. and Davis with the calibration of Johnson et al. since Johnson et al. states calibration at system initialization compensates for wide variations in individual device parameters (see section 0005).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CURTIS B. ODOM whose telephone number is (571)272-3046. The examiner can normally be reached on Monday- Friday, 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Curtis B. Odom/
Primary Examiner, Art Unit 2611
July 20, 2008

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/716,320	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	CURTIS B. ODOM	2611	